Hardware Reference Manual

Double-Density Floppy Disk Controller

Central Data Corporation

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1. General Information

The Central Data Double-Density Floppy Disk Controller board is designed to allow any Multibus* user to add 8" floppy disks to his system. The board operates with both single and double sided drives, but only operates in double-density mode in order to optimize the data seperator reliability. Up to four drives may be hooked to the controller, and the disk connector on the top of the board conforms to the industry standard Shugart Associates SA801/SA851 pinout.

The board uses the Western Digital FD1791 floppy disk controller chip as the interface to the disk. This part keeps track of the status of the drive being accessed, and formats processor commands to generate the proper disk interface signals. All transfers to and from disk occur by direct memory access (DMA), using standard bus arbitration as provided for in the Intel Multibus specification.

The board has a very reliable phase locked loop data seperator to regenerate the clock and data pulses from the disk drive during disk read operations. Since the board only operates in double-density mode, the seperator is optimized for that operation. A data seperator designed to operate in both single- and double-density modes causes a somewhat lower degree of reliability when recovering marginal data from the disk. To further increase reliability, a write precompensation circuit shifts the write data bits in a manner which will cause them to be read back at much closer to their nominal position than would have otherwise been the case. The recording format for the data on the disk is MFM (modified frequency-modulated).

The board requires eight I/O ports, four of which are used by the FD1791. The other four ports are used in output mode only, and they hold the starting DMA address and the drive/side select information. The addressing of the I/O ports can be on any eight port boundary using the full 16-bit I/O addresses called for in the Multibus specification. Optionally, 8-bit I/O addresses can be used.

The board can signal the completion of a command by driving an interrupt line on the Multibus, or the processor can poll a status register in the controller chip to determing when a command is finished.

* Multibus is a trademark of Intel Corporation and is used throughout this manual.

2. Functional Description

This section of the manual briefly describes the major sections of the board. The Principles of Operation section gives a detailed description of the schematics.

The first major section of the board consists of the disk interface, which contains the FD1791 floppy disk controller, the drive number select latch, and the buffers to the disk. Also in this section is a one-shot to provide proper head load timing. This guarantees that the controller will not try to read or write data until the head is fully settled after initially being loaded.

The next section is the write precompensation circuit, which shifts the write data bits as requested by the FD1791 to insure more reliable data storage. Each bit written can be shifted plus or minus 160ns of its nominal position before being sent to the disk. The 160ns value can be changed by changing potentiometers on the board.

The data seperator consists of a phase locked loop circuit which locks the FD1791's read clock to the read data coming from the disk. This circuit provides superior data reliability, due to its optimized double-density only design using a phase locked loop. Simpler digital counter techniques which work reliably for single density operation provide very poor performance in a double-density environment.

The Multibus interface consists of two sections: one where the processor board is accessing the disk controller as a slave device (when setting up a command or checking status), and the other where the board is operating as a bus master (doing a DMA operation with memory). The first section provides for address decoding for the I/O ports on the board, selection of the proper devices during I/O operations, and command acknowledgement to the processor. This section also has the driver for the interrupt lines of the Multibus which allows the board to signal the processor at the end of a command.

The second part of the Multibus interface contains all of the circuitry necessary to control the bus during DMA operations. Bus arbitration logic requests use of the bus

when the controller is ready for a transfer; address and data bus drivers properly access the memory location after the bus has been given to the board.

3. Principles of Operation

This chapter details the operation of the entire controller board. Any signal names in this text followed by a slash (/) indicate that the signal is active-low.

As in all Central Data schematics, a grid system is provided to help locate sources and destinations of signals. The source of any named signal will have references to all locations on the schematics where the signal is used. Each location where a signal is used, a reference is given to where it was generated.

If the location is on the same sheet as it is being referenced, it will show only a grid location (i.e. D2). If, however, the referenced signal appears on a seperate page, it will have the grid location preceded by the sheet number (i.e. 2-B5).

Furthermore, if a group of signals is commonly routed together, that group may be cross-referenced together. It is not necessary that all members of the group go to each destination listed, since the purpose of the cross-reference system is only to guide a user through the schematics.

Disk Interface

Sheet 1 of the schematics contains the interface to the floppy disk drives. The major circuitry on the sheet consists of the controller chip and the drive/head select latch.

The FD1791 floppy disk controller is used on the board to format processor commands to the disk. It keeps track of the head position on the disk, sends out MFM bit streams when writing data, and decodes read data using a phase locked loop generated clock. Full information concerning the programming and specifications of the FD1791 controller chip can be obtained from its manufacturer, Western Digital.

The processor/DMA interface to the controller consists of data bus buffers and selection circuitry. The data bus buffers consist of two 74LS242 bidirectional buffers (IC24 and IC25). Normally, these buffers gate data to the FD1791, with pins 1 and 13 high. If these pins go low (during a

processor or DMA read to the device), the data is gated from the FD1791 to the board's internal 8-bit data bus. Note that these buffers are inverting, required since the data pins of the FD1791 are active low.

The controller chip is selected when pin 3 goes low. If either pin 2 or pin 4 goes low during selection, a write or read will occur, respectively. The internal register that will be accessed is determined by the address inputs, pins 5 and 6. These registers are listed below:

Register	Read	Write
0	Status	Command
1	Track	Track
2	Sector	Sector
3	Data	Data

During DMA operations, when only the data register needs to be accessed, both address lines are forced high by the DMASEL inputs to the OR gates driving the address lines. When the processor is accessing the device, the buffered address lines from the Multibus are used to control the two pins.

A 2MHz clock drives the internal operations of the device, and the INIT/ signal clears internal flags and registers when the system is initialized. The DRQ output is used by the DMA circuitry to request another data transfer, and the FDINT signal can drive one of the Multibus vectored interrupt lines to signal command completion.

To interface to the disk drive connector, all outputs are buffered with open collector gates (IC2). Two inputs from the drives are buffered with inverters (IC8), while the other three inputs are routed direcly to the controller chip. The 74123 one-shot is used to provide head load timing to the FD1791. When the head is first loaded on the drive, the HLD signal goes high. This signal is buffered and triggers the one-shot, causing pin 4 of IC48 to go low. After 35ms, this output goes high, signaling to the controller that the head of the disk has been loaded and settled.

The drive/side select latch is IC45, with its three data inputs driven by the low-order bits of the internal data bus. This bus contains the Multibus data when the port is being written (when LATCH DRIVE is high). The 74S139 is used to decode the low-order two ouputs of the latch and select one drive out of four. The third output of the latch is buffered and sent directly to the disk connector. This signal can be used for double-sided drives to select the

side to be used.

Write Precompensation

Sheet 2 of the schematics shows the write precompensation circuitry. Also contained on the sheet is the master oscillator which drives the controller chip. The oscillator is a simple feedback network, with the resistors used to bias the 74S04 gates into their linear region, and the 100pf capacitor used to block any DC voltage to the crystal and to stabilize operation. After buffering, this 16MHz signal is divided down to 2MHz and used by the floppy disk controller chip.

The write precompensation circuit consists of several one-shots allowing for variable delays needed to operate with different drive types. When the board is shipped from the factory, Central Data sets the write precompensation amount to be 160ns, as specified by Shugart Associates for their drives. If other disk drives are to be used, that manufacturers literature should be consulted to determine if the write precompensation delay should be changed. If the difference is less than 20%, the board should not be changed.

The write data output from the FD1791 (WD) is buffered with a 74LS08, and used to latch the EARLY and LATE signals. These signals must be latched since they do not stay valid more than 125ns after the normal WD signal goes inactive. The outputs of the latches are labeled GATE EARLY and GATE LATE, while if neither output is high the GATE NOMINAL signal goes active, positioning the bit with no shift. Note that the precompensation is enabled only for tracks greater than 43, since both latches are held cleared on tracks 0-43.

The WD signal drives a chain of one-shots which time the precompensation delay. If the bit should be written early, the first output is used to generate the final output. If the bit should be written nominally, a delay is introduced from the position of early pulses to give the early bits a "backward" reference from nominal. Late bits are generated after a second delay, positioning them a "positive" amount from the nominal position. Figure 1 details the operation of the write precompensation delays. The one-shot used to drive COMP WD simply guarantees constant pulse widths to the disk, since all three inputs to it can be of different widths.

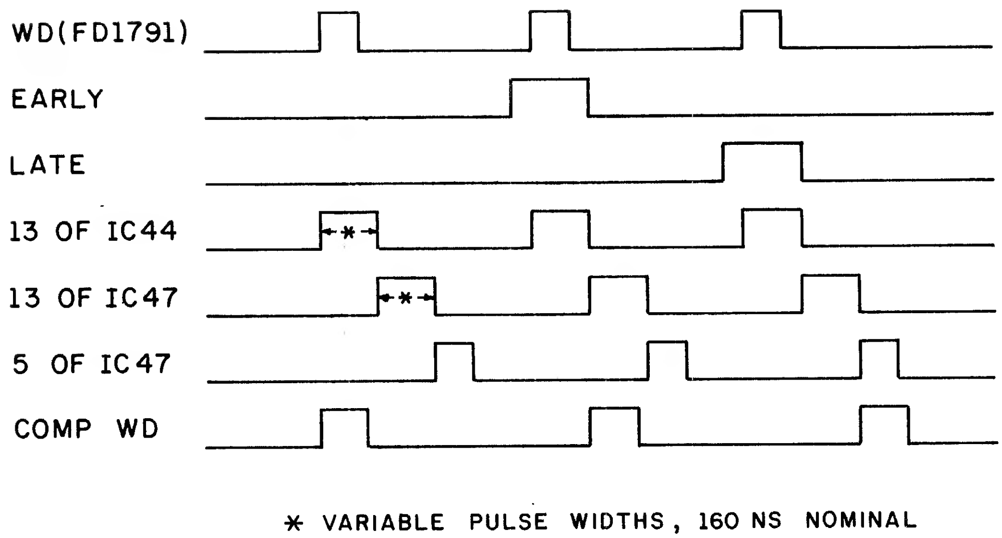


Figure 1. Write Precompensation Timing

Data Seperator

Sheet 3 of the schematics shows the phase locked loop data seperator circuitry. The circuit consists of a voltage controlled oscillator (VCO), phase detector, and input conditioner.

The voltage controller oscillator consists of the 74221 monostables (IC59) on the right side of the sheet. They are hooked up to form an oscillator, with the INIT/ signal used to guarantee startup during power-on. The 4.7K pot is used to set the free running frequency (when TRAN' is shorted low) to exactly 2MHz. The input to the circuit is the output of the op-amp, IC31. This op-amp doubles the input voltage on pin 3. Under stable conditions, this pin is biased to 2.5V with the 1M resistors. This causes an output voltage of 5V, under free running conditions, which is the normal value used by monostables for the timing resistor pullup. If this control voltage goes up, the period of the 2MHz VCO will go down (since the timing circuit will reach the monostables internal trigger voltage earlier). If the control voltage decreases, the reverse is true. This control voltage centers around 5V, going above or below this value only when the phase detector determins a frequency (period) change is needed.

The phase detector consists of the three gates to the left of the op-amp, along with the two 1N4148 diodes, the 1K and the 4.7K resistors. As shown in figure 2, the two inputs to the phase detector (TRAN and TRAN') have a nominal position

with respect to each other. If these signals stay related as shown (being 1/2 cycle of the 1MHz VCO apart), the loop will be locked. If the TRAN' signal ever sways from its nominal position, however, the phase detector will "pump up" or "pump down" the control voltage.

If the TRAN signal lasts more than 1/2 clock cycle after TRAN' goes active, it causes the "pump down" circuit to activate. If the TRAN signal lasts less than 1/2 clock cycle after TRAN', it causes the "pump up" circuit to activate. These signals cause the input to the op-amp to get lower or higher, in small increments each pulse. The R/C network on the input to the op-amp gives the circuit "memory" so that changes are not made instantly, and noise will not kick the system out of lock. Pin 12 of IC42, when low, causes the input to the op-amp to decrease, while when pin 8 of IC54 goes high, the input voltage increases. When the gates are not active, the 1N4148 diodes keep them isolated from the voltage biasing circuit.

The input conditioning circuit takes the read data from the disk (RD DATA), and generates 175ns RAW READ/ pulses for the FD1791. The 74221 after this pulse generator has a 1us output for each read data pulse. The 74LS74 is used to latch the sampled phase shift for processing in the phase detector circuit.

The remaining circuitry on this sheet divides the 2MHz VCO signal to a 1MHz signal (used by the phase detector circuit) and a 500KHz signal which is used by the FD1791. Also on the sheet is the divider for the 16MHz oscillator and the FD1791 read/write enable gates which combine processor I/O requests and DMA read/write requests.

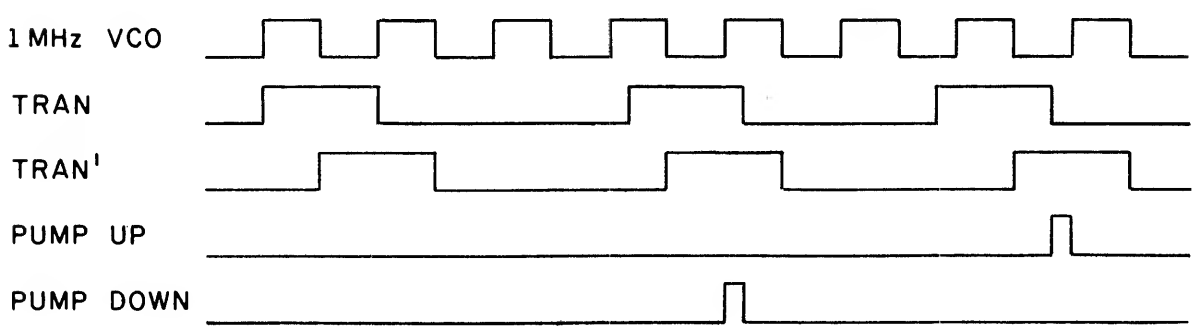


Figure 2. Data Seperator Timing

Bus Interface: Slave Operation

The board requires the use of eight of the system's I/O ports. These ports can be started on any eight port boundary, using either 8- or 16-bit addresses.

All of the address lines from the Multibus are buffered through 74LS04 gates. The buffered address lines are then routed to address decoding circuitry (A3-A15) and to chip selection circuitry (A0-A2).

The address decoding circuit consists of eleven 74LS266 open collector exclusive-NOR gates. All of the outputs of the gates are tied together, allowing any of the gates to pull the output low if its inputs do not match. If all of the pairs of inputs match, the common output is pulled high by a resistor to +5V.

One input from each of the gates goes to a buffered address line, with the other going to a dip-switch. This dip-switch, when closed, causes the corresponding gate input to become grounded. Under this circumstance, the address line leading to the same gate must also be low for the board to be addressed. If the switch position is left open, the input to the gate goes to a high state, thus comparing for a high address line.

To allow the selection between 8- and 16-bit I/O addressing, the outputs of the gates related to A8-A15 are connected through a shorting plug to the outputs of the gates related to A3-A7. If the shorting plug is installed, then the board decodes the full 16-bit address bus. If the shorting plug is removed, then the upper eight gates will not drive the common output, and thus only the lower five lines (A3-A7) are used for addressing.

When the address comparator is equal, pin 4 of IC9 will go high. When this pin is high, and the system is doing an I/O operation the BOARD SEL line goes high. When this line and BA2 are high the 74S139 is enabled, using the lower two address lines to select which auxillary port should be written. These ports consist of the DMA address registers as well as the drive/side select latch.

If BA2 is low and the address comparator is equal, pin 8 of IC9 goes high. When this is high or the board is doing a DMA operation the FDCS/ signal will go low, enabling the FD1791. Note that the RE/ or WE/ inputs to the controller are needed to actually transfer data, and their generation was discussed earlier.

The board generates two command acknowledge signals. The

first, XACK, indicates when a data transfer is complete and the processor can go to the next cycle. The other, AACK, gives the processor advance information related to when a transfer will be complete.

The circuit which generates the acknowledge signals consists of a shift register (74LS164, IC14) which is kept cleared when the board is not active. When an I/O command occurs, the clear input goes high, allowing the register to shift 1's through at the BCLK rate. The eight outputs of the shift register, which go high from 100-800ns after the time a command starts, can be jumpered to the XACK and AACK drivers (IC15). Note that since the command is asynchronous with respect to the bus clock the outputs may vary up to one clock cycle (i.e. the second output can occur anywhere from 100-200ns after command initiation).

The user can also select either acknowledge signal to be returned as soon as the board is selected by tying the driver's input high. The drivers are enabled whenever a command is occuring to this board, thus gating the proper timing onto the bus.

The data bus buffers consist of two 74LS242s (IC39 and IC40) on sheet 6, each one buffering four data lines. These are inverting buffers, thus immediately correcting for the inverted data on the bus. Since the directional enable pins of the buffers are of opposite polarity, they can be tied together, and are driven by a signal (pin 1 of IC60) which goes low whenever the CPU is doing an I/O read to the FD1791, or when the board is acting as a bus master and writing data to memory. During all other conditions, this signal is high, sending data from the Multibus into the board.

Bus Interface: Master Operation

Sheet 5 of the schematics shows the DMA control circuitry. This circuitry gains control of the bus whenever an access is required, and drives the address, data, and memory command lines when it has control. DMA operations are started when the DRQ signal from the FD1791 goes high. All bus operations are done synchronously with the bus clock (BCLK). Full information concerning the multi-master capabilites of the Multibus should be referred to the Intel Multibus specification. Figure 3 shows the timing for a DMA read, with figure 4 showing a DMA write cycle.

When a DRQ comes from the controller, it is synchronized with the bus clock by clocking pin 3 of IC6 when BCLK is high. This guarantees the setup time of the next flip-flop, which is used to generate the DMARQ signal to the bus. On

the first BCLK cycle after the bus is requested and the BUSY/ signal is high along with BPRN, bus control is taken. The DMASEL signal signals when this board has control of the bus. The DMA read and write timing circuits are different, and will be discussed in the next two paragraphs.

When the board gains control of the bus and needs to do a read operation to the bus (a write operation to the disk--FDWR high), the 74LS164 counter (IC67) is allowed to shift 1's through (at the BCLK rate). The first output (on the first BCLK after DMASEL goes high) causes the memory read command line to go active. This also disables further counting until the XACK signal (which has been synchronized to the BCLK) is returned by the memory board, indicating that the read data is valid on the Multibus. When this occurs, the next BCLK allows the DMAWR signal to be clocked high. This starts a write to the FD1791. After five more BCLK cycles, the END WR DMA/ signal goes low, causing the cycle to end and the bus to be released.

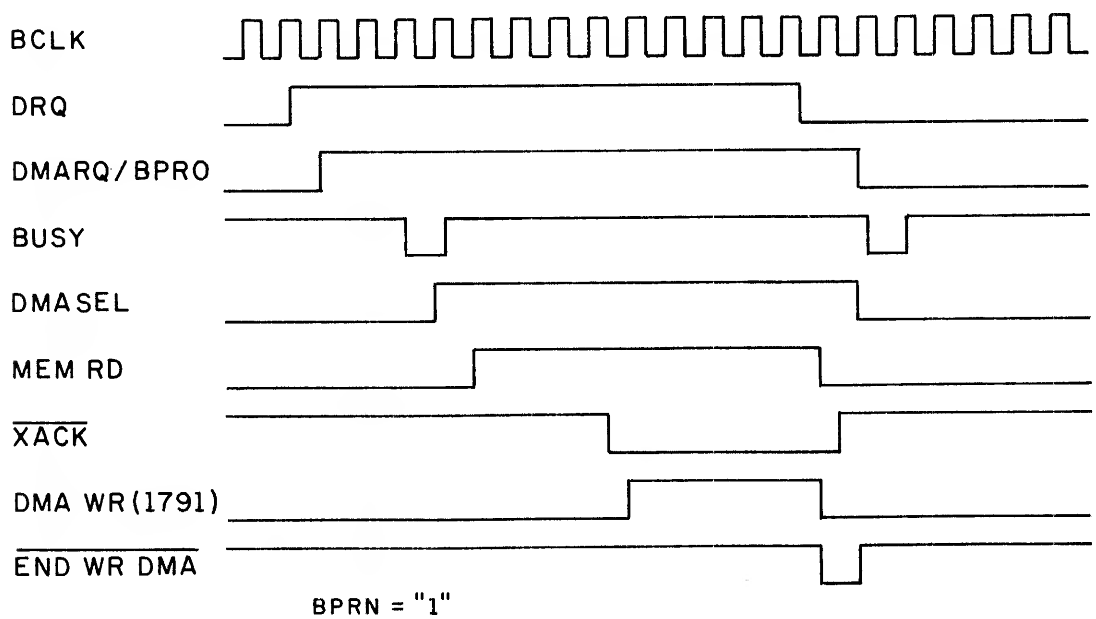


Figure 3. DMA Read Timing

When the board needs to do a write cycle to the bus, it allows IC63 to clock through 1's. When the clear input to this device is raised, the read enable input to the FD1791 is made active (using DMARD), causing the data register's outputs to appear on the Multibus after 400ns. After four clock cycles, the MEMWRT signal goes active, allowing a memory write cycle to start on the bus (since the data is now setup). When this occurs, the clock to the shift

register is inhibited until the XACK is returned by the memory board, which allows the END RD DMA/ signal to finish this bus cycle.

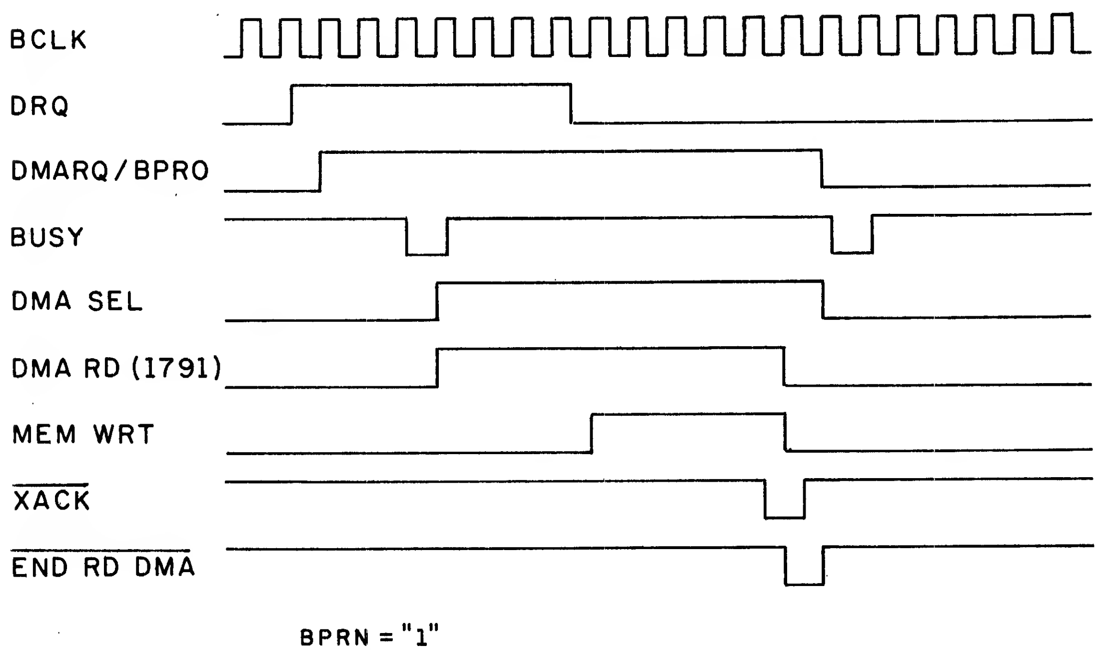


Figure 4. DMA Write Timing

Sheet 6 of the schematics shows the address counter and address bus drivers. The address counters consist of four 74LS163's which are incremented after every DMA cycle (when CLK ADR goes high). The high-order address lines (A16-A23) do not increment during DMA operations, since they are simply the outputs of a latch (IC64).

To load the addresses before a DMA operation, the following procedure must be followed to properly latch the addresses. This code guarantees that the clock pins of the counters will pulse during the output operation.

```
*
*    Z8000 CODE TO SETUP B1015 ADDRESS REGISTERS
*    RR4 HAS THE START ADDRESS NEEDED ON ENTRY
*
ADR     LD        R0,#0FFF
        OUTB      ADR0,RH0       SETUP CARRY OUTPUTS
        OUTB      ADR0,RL0       OF 74LS163s
        OUTB      ADR1,RH0
        OUTB      ADR0,RH0
        OUTB      ADR0,RL0
        OUTB      ADR1,RH5       SEND OUT MIDDLE BYTE
        OUTB      ADR0,RH0
```

```
OUTB      ADR0,RL5      SEND OUT LOW BYTE
XOR       RH4,#FF       INVERT FOR HIGH BYTE
OUTB      ADR2,RH4      SEND IT OUT
RET       UN            RETURN
```

4. Installation/User Selectable Options

This section of the manual describes how to install the board into the Multibus system. Note that all potentiometers on the board should be left unchanged, unless the system designer determines that they need to be adjusted (due to unusual system circumstances).

System Board Location

The disk controller board must be placed in the proper card position of the system in order to resolve its priority with other bus masters. In a serial bus priority resolution circuit, one designated position in the mother board has the highest priority, with positions of decreasing priority moving away from that location. In this situation, the highest priority boards (such as disk controllers, etc.) are placed in the first positions, with the CPU board(s) placed next, and any lower priority boards placed after the CPU(s). Since there are no fixed rules for determining the relative priority of various types of boards, it is left to the system designer to determine this. Most Central Data designed systems have boards inserted in the following priority:

Cartridge/Winchester Disk Controllers
Floppy Disk Controllers
Intelligent I/O Boards
CPU Boards

In systems utilizing parallel bus priority resolution circuitry, the priority of each card position is determined by a special priority resolver. Since every system can be designed differently, the system designer will have total responsibilty for determining the locations of each type of board.

Addressing

The board has two dip switches used to select the port addresses it will respond to. Each switch position corresponds to one address line, from A3 to A15. As marked on the board, A15 is selected by the left-most switch, while A3 is selected by the right-most. An address line is compared for "0" if the switch is closed (up), as printed on

the board. With the switch left open (down), the corresponding address line is compared for "1".

If 16-bit I/O addressing is to be used, a shorting plug must be placed over the two wire-wrap pins marked EXTENDED I/O. For systems where only 8-bit I/O addressing is used, this shorting plug should be left off. Also, for 8-bit systems, the upper eight address switches are not used.

XACK and AACK Generation

In order for the board to acknowledge processor commands to it, two lines are provided to indicate when a data transfer is complete. The XACK (transfer acknoweledge) line is driven by the board when the transfer is completely finished, and the processor is allowed to complete the cycle. The AACK (advanced acknowledge) is provided to allow systems to operate at their full speed potential (by preventing wait states), since it can be returned before XACK. Only XACK is used to indicate when a cycle can end, with the function of AACK to give advance information concerning the timing of the board.

Both of the lines can be strap selectable to return to the processor from 0-800ns after a command is received, in 100ns increments. The selection of timing for each line is done with shorting plugs placed over wire-wrap pins on the board.

The board has two rows of wire-wrap pins which are used for XACK/AACK generation. The top row is used for XACK, while the bottom row is for AACK. Each row consists of 9 pairs of pins, with each pair being one timing combination. To setup the board, the user needs to place a shorting plug in each row, under the timing number which he desires.

The timing numbers are marked to be the maximum return time for the signal involved (multiplied by 100ns). The minimum time is 100ns below the maximum time. For example, the pins marked "4" will return their signals from 300-400ns after a command is received. The pins marked "0" always return the signal immediately.

Since the XACK timing is tied to the access time of the board, the setting of that plug is suggested to be "5". The setting of the AACK strap will have to be determined by the system designer, using the information presented here.

One note--the timing for both acknowledge lines is dependent on the BCLK (bus clock) signal from the Multibus. It is assumed here that this clock is running at 10MHz, so if any other frequency is used on the system, the spacing between strap postions will be the period of the actual clock rather

than 100ns. For example, a system with a 9.5MHz CCLK signal will have 105ns strap selection spacing.

Interrupt Selection

The user can cause the board to drive any of the eight vectored interrupt lines on the Multibus when any command is completed. A shorting plug must be placed on the wire-wrap pins corresponding to the interrupt level that the user desires. If no interrupt is to be generated, then no minijump should be placed in the interrupt selection area of the board.

INITIAL SETTINGS:

XACK :5.
AACK :1.
INT :6.
EXTENDED I/O : IN.
IC17 : ØØØØ ØØØØ.
IC18 : ØØ1ØØ.
IC19 : OUT.
IC16 : OUT
ADDRESS ≡ HEX ØØ2Ø — HEXØØ27

5. Specifications

Word Size

8 bits

Addressing

This board requires eight I/O ports. The base address of these ports can be on any eight port boundary. Depending on strap selection, either 8- or 16-bit addresses can be used for I/O addressing.

The eight ports used are defined as follows:

Address	Input Function	Output Function
0	Floppy Status	Floppy Command
1	Track Register	Track Register
2	Sector Register	Sector Register
3	Data Register	Data Register
4	not used	DMA A0-A7
5	not used	DMA A8-A15
6	not used	Inverted DMA A16-A23
7	not used	Drive/Side Select

Data Transfer Rate

62,500 bytes per second

Disk Drive Connector

Conforms with Shugart Associtate SA801/SA851 specifications (50 pin, .1" spacing).

Access Time

450ns, maximum

Interrupt Capabilities

Whenever a command is completed (with or without error) an interrupt can be generated on any of the eight Multibus interrupt lines.

Interface

All P1 signals meet the IEEE Multibus proposed specification. Additionally, four lines on P2 are defined as shown below to allow a full 24-bit address bus:

P2 Pin	Function
57	A20
58	A21
59	A22
60	A23

Electrical Characteristics

Vcc= +5V $\pm$5%
Vdd= +12V $\pm$5%
Icc= 1.1A typ, 1.6A max
Idd= 0.01A typ, 0.04A max

Environmental Characteristics

Operating Temperature: 0 C to +55 C
Relative Humidity: 0 to 90% (non-condensing)

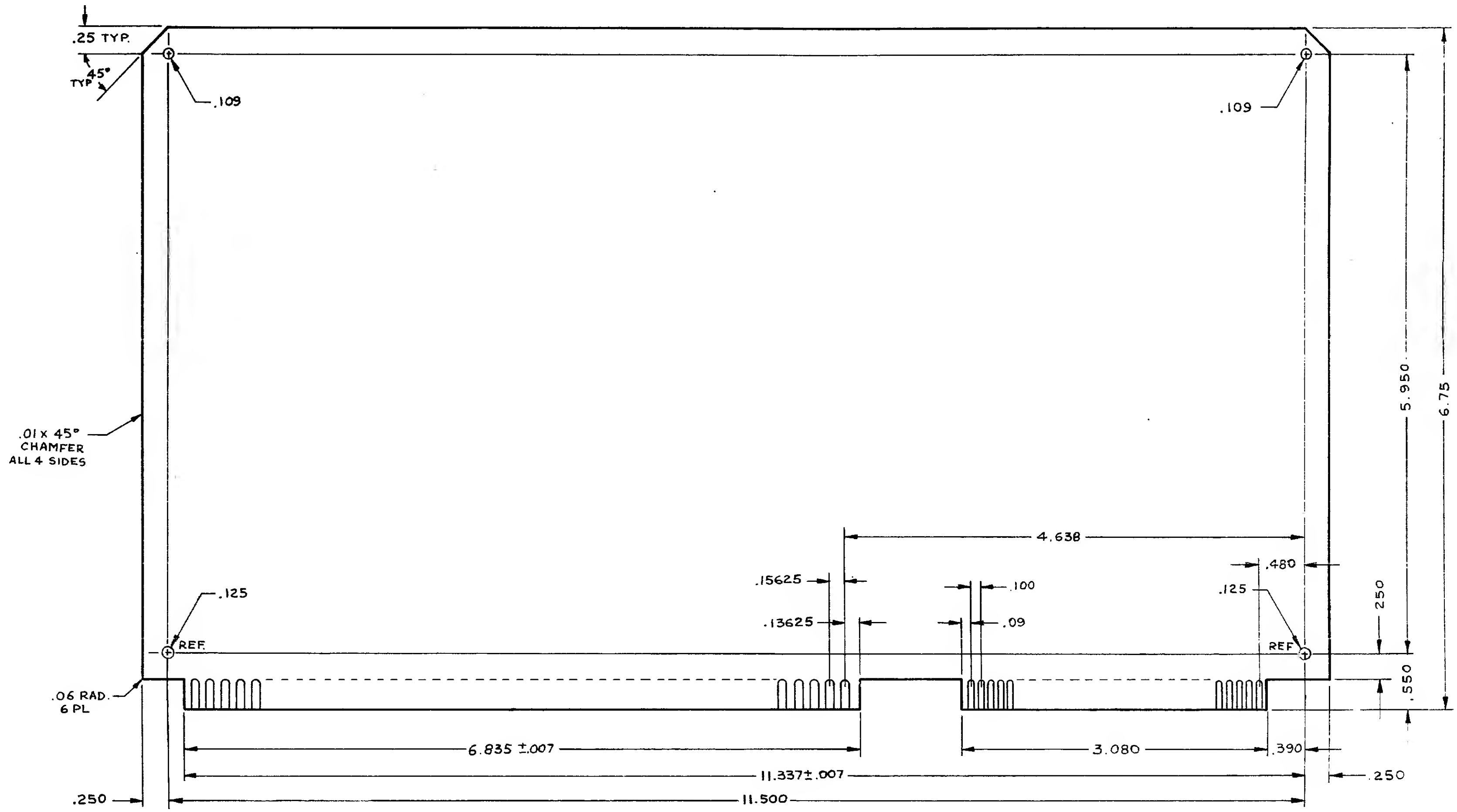
Physical Characteristics

Dimensions: see the basic Multibus dimensions on the following page. The connector for the disk is 2.58" wide, and its right edge is 4.46" from the center of the right-hand reference hole.

Weight: 9 oz (255gm)

Ordering Information

Part Number: B1015
Description: Multibus Double Density Floppy Disk Controller



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NO.

SHEET OF

MULTIBUS BOARD DIMENSIONS

6. Software Driver Routines

The following pages show example driver routines written in Z8000 code. The routines are general purpose in nature, and are not meant to be used directly in any particular application.

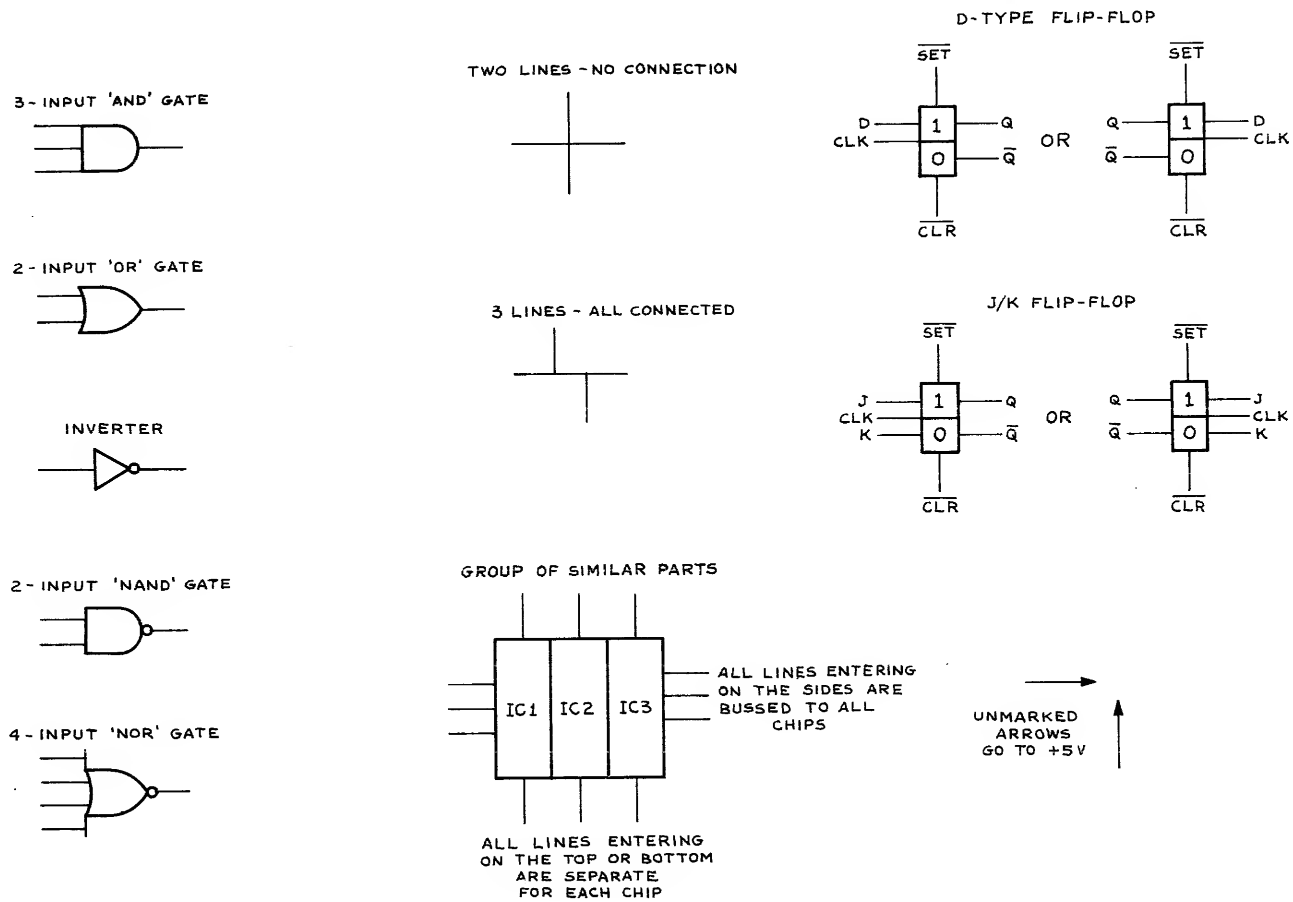
```
ADDR    B1 B2 B3 B4 LABEL  OPCODE     OPERAND    COMMENTS

000000              UN     EQU        8
000000              Z      EQU        6
000000              NZ     EQU        E
000000              CY     EQU        7
000000              NC     EQU        F
000000              PL     EQU        D
000000              MI     EQU        5
000000              NE     EQU        E
000000              EQ     EQU        6
000000              OV     EQU        4
000000              NOV    EQU        C
000000              GE     EQU        9
000000              LT     EQU        1
000000              GT     EQU        A
000000              LE     EQU        2
000000              UGE    EQU        F
000000              ULT    EQU        7
000000              UGT    EQU        B
000000              ULE    EQU        3
000000              *
000000              FORM   EQU        0C
000000              CR     EQU        0D
000000              LF     EQU        0A
000000              BS     EQU        08
000000              ESC    EQU        1B
000000              CCPY   EQU        10
000000              CONX   EQU        18
000000              *
000000              FLGS   EQU        01
000000              FCW    EQU        02
000000              REF    EQU        03
000000              PSEG   EQU        04
000000              POFF   EQU        05
000000              NSEG   EQU        06
000000              NOFF   EQU        07
000000              *
000000              CRY    EQU        08
000000              ZRC    EQU        04
000000              SGN    EQU        02
000000              PV     EQU        01
000000              ALL    EQU        0F
000000              *
000000              DCOM   EQU        20         DISK COMMAND REGISTER
000000              DSTA   EQU        20         STATUS REGISTER
000000              DTRK   EQU        21         TRACK REGISTER
000000              DSEC   EQU        22         SECTOR REGISTER
000000              DDAT   EQU        23         DATA REGISTER
000000              ADR0   EQU        24         LOW ADDRESS
000000              ADR1   EQU        25         MIDDLE ADDRESS
000000              ADR2   EQU        26         HIGH ADDRESS
000000              DRV    EQU        27         DRIVE/SIDE SELECT LATCH
000000 00 00        TFLG   SAVE       2          FLAG TELLING IF COMMAND IS PENDING
000002 00 00        LSTA   SAVE       2          LAST STATUS (ERROR BITS)
000004              *
000004              *      THIS ROUTINE IS CALLED WHEN A PROGRAM WANTS TO START A FLOPPY
```

```
LINE  ADDR   B1 B2 B3 B4 LABEL  OPCODE    OPERAND     COMMENTS

      000004             *      DISK COMMAND.  THE FOLLOWING REGISTERS SHOULD BE LOADED BEFORE
      000004             *      CALLING THE ROUTINE:
      000004             *
      000004             *      RR2       STARTING TRANSFER ADDR
      000004             *      RH4       TRACK
      000004             *      RL4       SECTOR
      000004             *      RH5       DRIVE/SIDE
      000004             *      RL5       COMMAND
      000004             *
      000004             *      THE ROUTINE RETURNS WHEN THE COMMAND IS COMPLETE, AND HAS THE
      000004             *      ERROR STATUS OF THE OPERATION IN RL0.  THIS BYTE IS ZERO IF NO
      000004             *      ERRORS OCCURED, AND THE FOLLOWING BITS ARE SET FOR ERROR CONDITIONS:
      000004             *
      000004             *      BIT 2     LOST DATA
      000004             *      BIT 3     CRC ERROR
      000004             *      BIT 4     SEEK ERROR/RECORD NOT FOUND
      000004             *      BIT 5     WRITE FAULT
      000004             *      BIT 6     WRITE PROTECT
      000004             *      BIT 7     NOT READY
      000004             *
      000004 4D 06 80 00 FCOM   TSET      <^TFLG>TFLG    INDICATE COMMAND IN PROGRESS
      000008 00 00
      00000A 21 00 0F FF        LD        R0,#0FFF
      00000E 3A 06 00 24        OUTB      ADR0,RH0    SETUP COUNTERS TO RECEIVE ADDRESSES
      000012 3A 86 00 24        OUTB      ADR0,RL0
      000016 3A 06 00 25        OUTB      ADR1,RH0
      00001A 3A 06 00 24        OUTB      ADR0,RH2
      00001E 3A 86 00 24        OUTB      ADR0,RL0
      000022 3A 36 00 25        OUTB      ADR1,RH3    SEND MIDDLE ADDRESS
      000026 3A 06 00 24        OUTB      ADR0,RH0
      00002A 3A B6 00 24        OUTB      ADR0,RL3    SEND LOW ADDRESS
      00002E 09 02 00 FF        XOR       RH2,#FF     HIGH ADDRESS MUST BE INVERTED
      000032 3A 26 00 26        OUTB      ADR2,RH2    SEND IT
      000036 3A 46 00 21        OUTB      DTRK,RH4    TRACK
      00003A 3A C6 00 22        OUTB      DSEC,RL4    SECTOR
      00003E 3A 56 00 27        OUTB      DRV,RH5     DRIVE/SIDE
      000042 3A D6 00 20        OUTB      DCOM,RL5    START THE COMMAND
      000046 4D 04 80 00 FCM2   TEST      <^TFLG>TFLG   SEE IF COMMAND DONE
      00004A 00 00
      00004C EE FC              JR        NZ,FCM2     NO
      00004E 30 08 FF B0        LDRB      RL0,ISTA    GET STATUS BYTE
      000052 06 08 FC FC        ANDB      RL0,#FC     MASK OFF DRQ, BUSY
      000056 8D D4              TEST      RL5         SEE IF TYPE 1 COMMAND
      000058 E5 02              JR        MI,FCM3     NO
      00005A 06 08 BB BB        ANDB      RL0,#BB     TAKE OUT WRITE PROTECT AND TRK 0
      00005E 06 0D E0 E0 FCM3   ANDB      RL5,#E0     SEE IF READ SECTOR
      000062 0A 0D 80 80        CPB       RL5,#80
      000066 9E 0E              RET       NE
      000068 07 08 00 DF        AND       RL0,#DF     MASK OFF RECORD TYPE
      00006C 9E 08              RET       UN
      00006E             *
      00006E             *      THIS ROUTINE SHOULD BE CALLED WHEN THE FLOPPY DISK CONTROLLER
      00006E             *      INTERRUPTS.
      00006E             *
      00006E 93 E0       INT    PUSH      @RR14,R0
```

```
LINE  ADDR   B1 B2 B3 B4 LABEL  OPCODE     OPERAND    COMMENTS

0111  000070 3A 84 00 20        INB        RL0,DSTA     READ STATUS, CLEAR INTERRUPT
0112  000074 32 08 FF 8A        LDRB       LSTA,RL0
0113  000078 4D 08 80 00        CLR        <^TFLG>TFLG    DONE WITH COMMAND
0114  00007C 00 00
0115  00007E C8 20              LDB        RL0,#20
0116  000080 3A 86 F0 01        OUTB       F001,RL0     CLEAR ISR OF 8259A ON Z8000 BOARD
0117  000084 97 F0              POP        R0,@RR14
0118  000086 7B 00              IRET
```

7. Schematics

The following pages contain the schematics for the Double-Density Floppy Disk Controller board. A full description of the circuitry is given in the Principles of Operation section of this manual.



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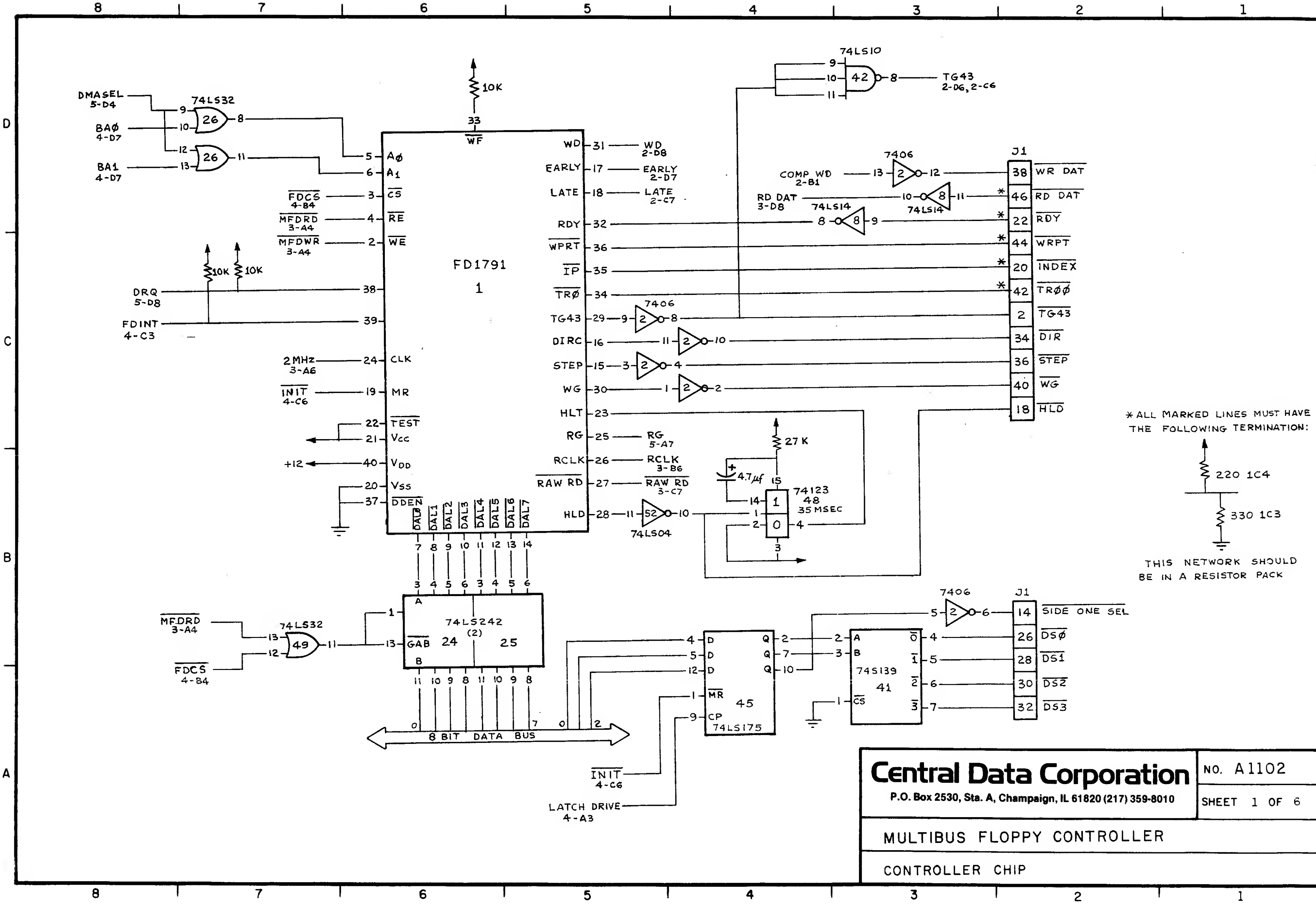
DRAWING CONVENTIONS



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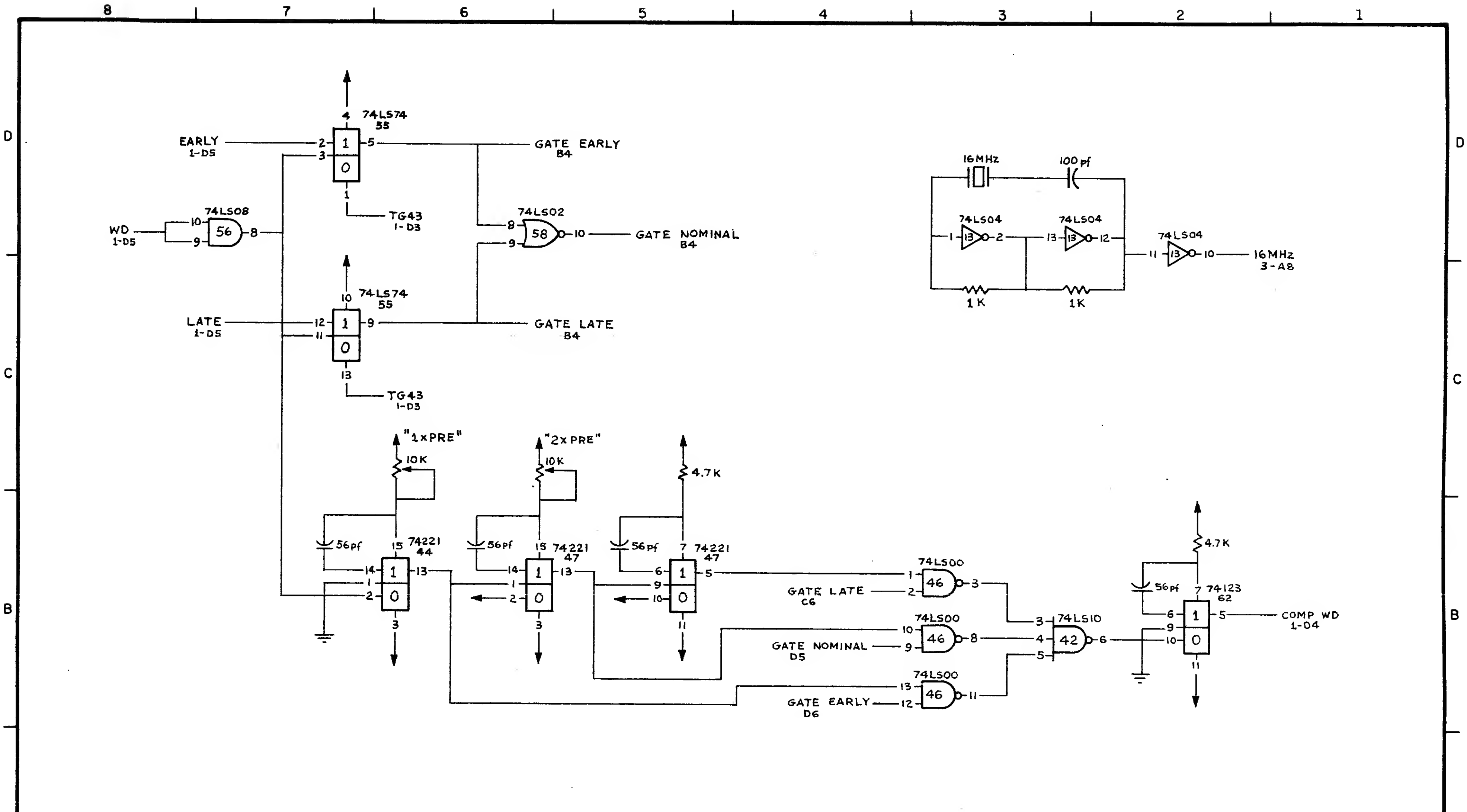
SHEET 1 OF 6

MULTIBUS FLOPPY CONTROLLER

CONTROLLER CHIP



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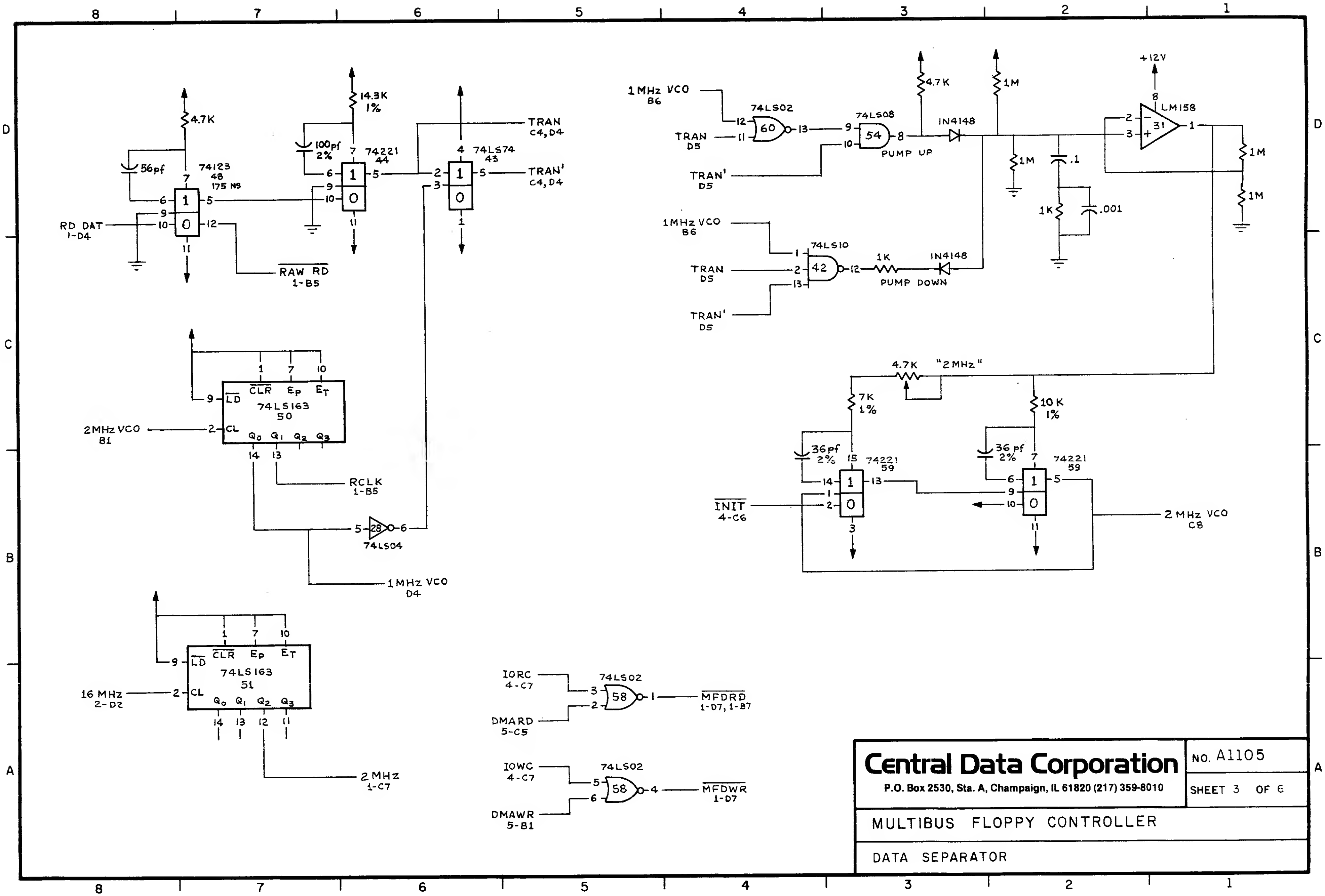
SHEET 2 OF 6

MULTIBUS FLOPPY CONTROLLER

WRITE PRECOMP



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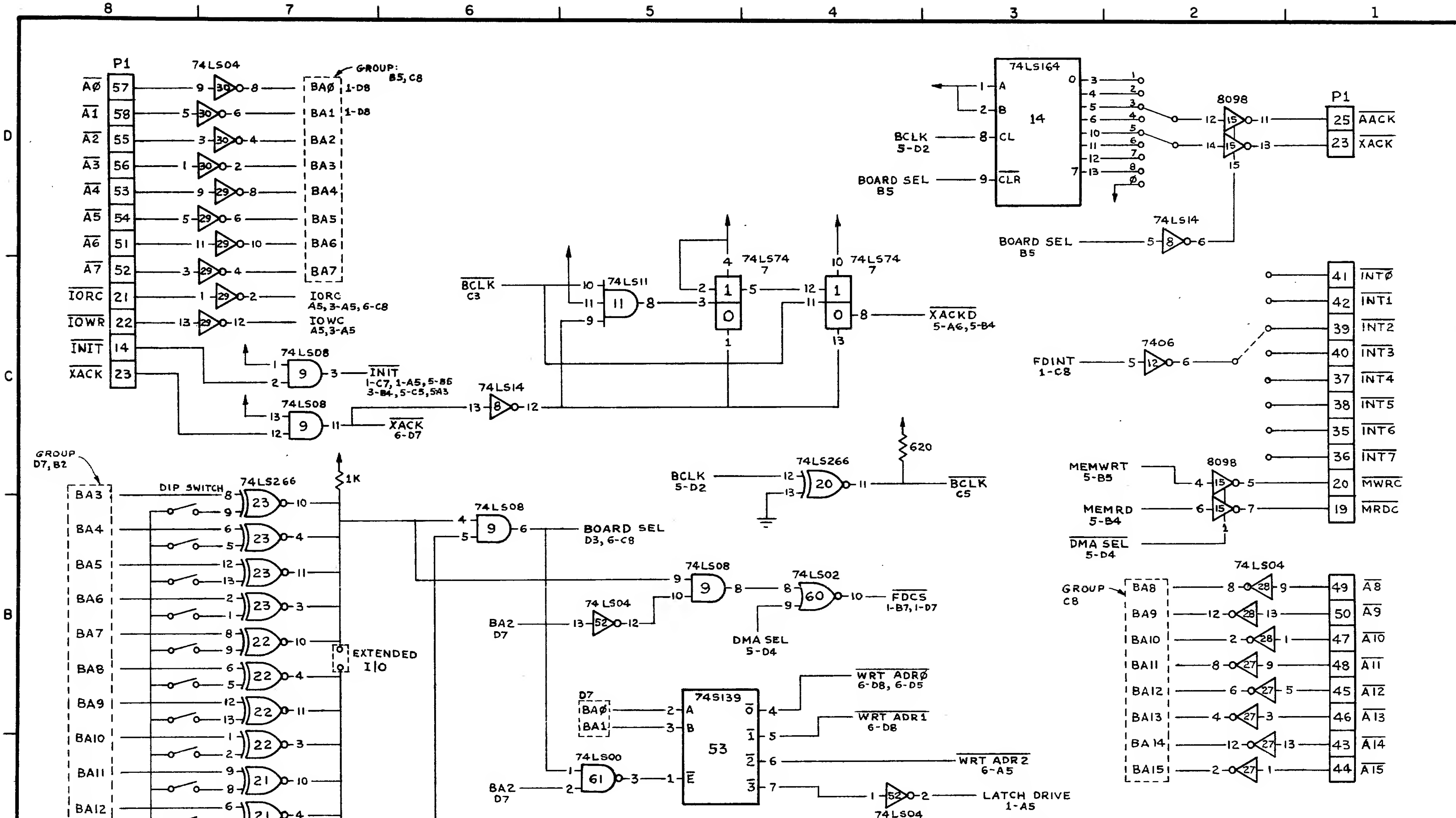
SHEET 3 OF 6

MULTIBUS FLOPPY CONTROLLER

DATA SEPARATOR



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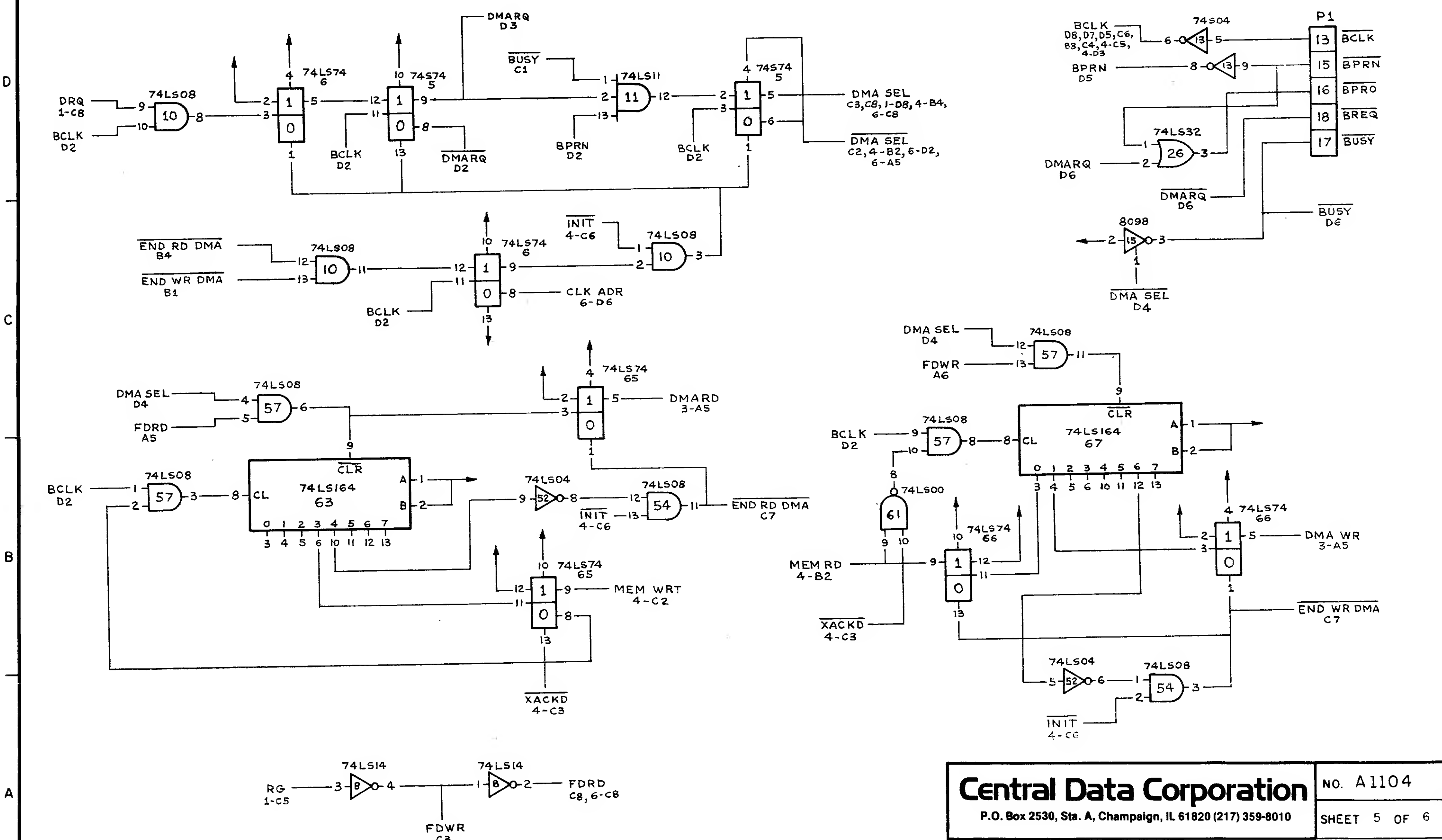
NO. A1106

SHEET 4 OF 6

MULTIBUS FLOPPY CONTROLLER

ADDRESSING



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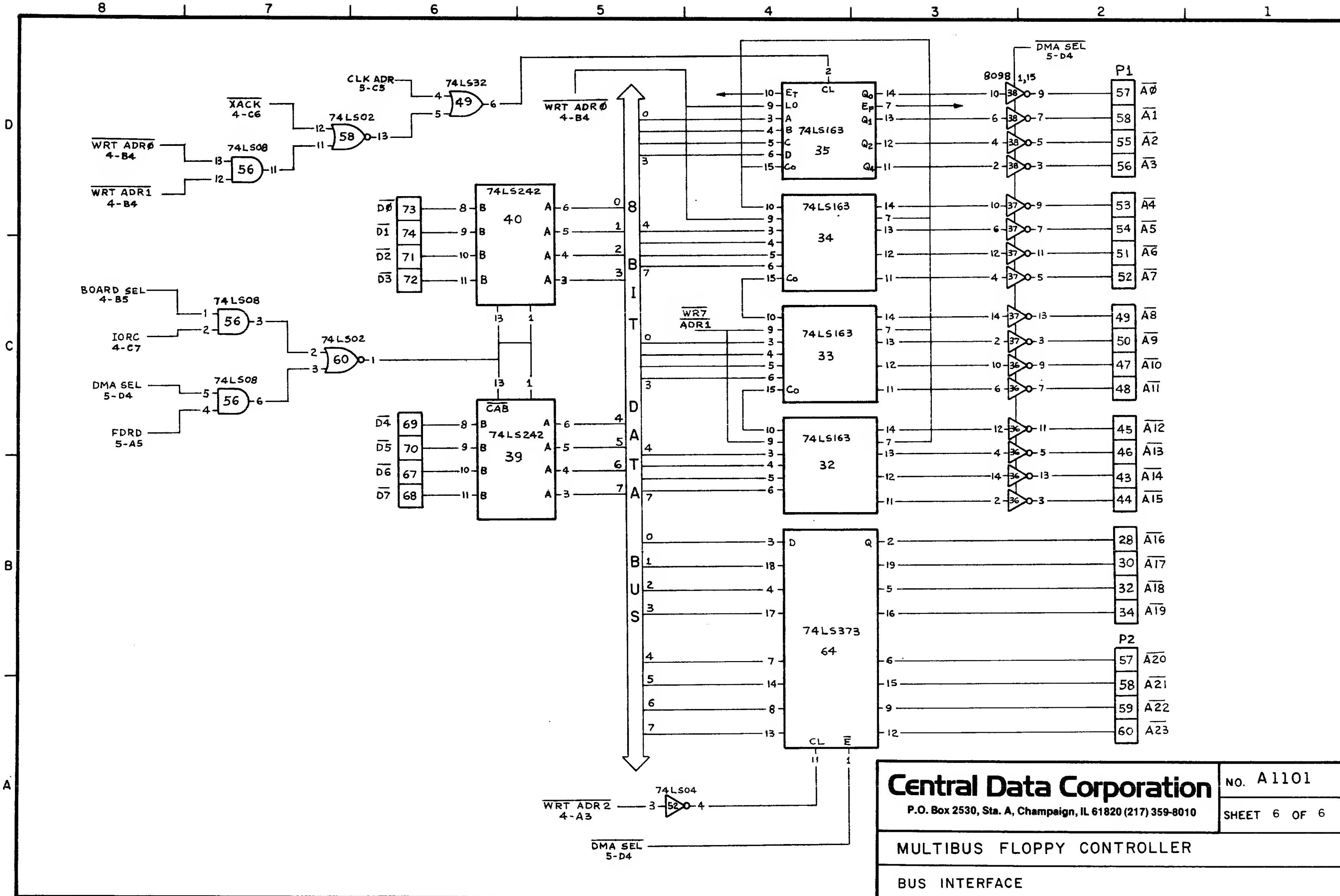
SHEET 5 OF 6

MULTIBUS FLOPPY CONTROLLER

DMA CIRCUITRY



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NO. A1101
SHEET 6 OF 6

MULTIBUS FLOPPY CONTROLLER

BUS INTERFACE